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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,727	12/08/2003	Ian M. Williams	NVDA/P000737	3949

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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,727	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *15-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 31-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-14, 31-35 in the reply filed on May 7, 2007 is acknowledged. Accordingly, claims 17-22, 24-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 5-11, 14, 31, 33, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Simmonds et al. (U.S. Patent No. 6,646,654).

As per claim 1, Simmonds et al. teach a method for synchronizing two or more graphics processing units (Fig. 3), comprising:

receiving a clock signal from a clock generator (*such as Reference clock oscillator 120, Fig. 5*) of a first graphics processing unit and an external synchronization signal (104);

determining whether the phase of the clock signal and the phase of the external synchronization signal are synchronized;

adjusting the frequency of the clock generator to the frequency of the external synchronization signal if the phases of the clock signal and the external synchronization

signal are not synchronized to generate a synchronized timing signal (*this is inherently done by the PLL 130, see attached definition of "phase locked loop"*);

transmitting the synchronized timing signal to a second graphics processing unit; and

producing an image for synchronous output to multiple displays using the synchronized timing signal (*see disclosure of Figs. 3, 5, and 8*).

As per claim 2, Simmonds et al. teach transmitting the synchronized timing signal from the second graphics processing unit to a third graphics processing unit (Fig. 3).

As per claim 5, Simmonds et al. also teach synchronizing a swap ready signal of the second graphics processing unit with a swap ready signal of the first graphics processing unit (col. 9, lines 56-67).

As per claim 6, although not explicitly, Simmonds implicitly teach

receiving a frame divider (since Simmonds teach image spans across multiple PC systems discussed in the Background of the Invention);

triggering a new video start address in a memory; and

determining whether a swap ready element on at least one of the graphics is logically true (Fig. 10 and its disclosure).

As per claim 7, although not explicitly, Simmonds implicitly teach scanning out data from the memory starting at the new video start address if the swap ready element on the at least one of the graphics processing units is logically true (so that all the graphics processing units receive new frame, and also to prevent race hazard).

As per claim 8, Simmonds further teach determining whether the current scanline is within a video blanking interval; and

scanning out the data from the memory starting at the new video start address if the sap ready element on the at lest one of the graphics processing units is logically true and the current scanline is within the video blanking interval (inherently because this is the time the graphics processing units are ready to receive the new frame).

As per claim 9, as cited above in claim 7, since Simmonds teach scanning out data from the memory if the swap ready element on the at least one of the graphics processing units is logically true, it is also implied that a series of video memory block transfers are performed.

Claim 10, which is similar in scope to claim 8, is thus rejected under the same rationale.

As per claim 11, Simmonds teach the swap ready element is logically true when an image content stored in a back portion of a frame buffer in the at least one of the graphics processing units is ready to be transferred to a front portion of the frame buffer (col. 2, lines 33-39).

As per claim 14, Simmonds teach the first and second graphics processing units are implemented on a printed circuit board (i.e. in the same chassis, col. 4, lines 3-5).

Claim 31, which is similar in scope to claim 1, is thus rejected under the same rationale.

Claim 33, which is similar in scope to claim 5, is thus rejected under the same rationale.

As per claim 34, which is similar in scope to claim 1 because Simmonds teach the plurality of graphics processing units are configured in a daisy chained manner (Fig. 3).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmonds et al. (U.S. Patent No. 6,646,654).

As per claims 12 and 13, although Simmonds does not explicitly teach the swap ready element is logically true when a voltage on the swap ready element is in a logical HIGH/LOW state, Simmonds does teach generating and transmitting buffer swap ready signal to the graphics processing units (see also col. 10, lines 53-67). Therefore, it would have been obvious to one skilled in the art to implement the generated buffer swap ready signal using voltage with a logical HIGH/LOW state, because LOW or HIGH voltage state is commonly used to determine or activate a logic state in any circuit design.

6. Claims 3, 4, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmonds et al. (U.S. Patent No. 6,646,654) in view of Deering et al. (U.S. Patent App. No. 2004/0012600)

As per claim 3, Simmonds et al. fails to teach synchronizing a first stereo field of the first graphics processing unit with a second stereo field of the second graphics processing units. However, Simmonds does teach adjusting the phase of the video signal of the second graphics processing unit to that of the first graphics processing unit as cited above. Deering et al, as cited in the previous Office Action teaches synchronizing stereo fields of video signal.

Therefore, it would have been obvious to one skilled in the art to modify the video signal as taught by Simmonds by stereo images as is taught by Deering et al. so that synchronization as taught by Simmonds can be used with other video signals, such as stereoscopic video.

Claim 4, which is similar in scope to claim 2, is thus rejected under the same rationale.

Claim 32, which is similar in scope to claim 3, is thus rejected under the same rationale.

7. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Simmonds et al. (U.S. Patent No. 6,646,654) in view of Itaki et al. (U.S. Patent No. 6,900,844, Itaki, hereinafter).

As per claim 35, Simmonds fails to teach a means for indicating visually that the synchronization timing signal is transmitted from the first graphics processing unit to the second graphics processing unit. However, Itaki teaches this feature. As shown in Fig. 1, Itaki teaches a method of synchronizing a plurality of graphics processing units 11-13, each graphics processing unit includes an indicator 5 (Fig. 2), for displaying the synchronizing timing signal from the first graphics processing unit to the second graphics processing unit (Figs. 6 and 7, and their disclosures). Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Itaki in combination with the method as taught by Simmonds in order to allow all of video to be synchronized in the same display pattern (col. 10, lines 37-60).

Response to Arguments

8. Applicant's arguments with respect to claims 1-14, 31-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen

07/11/2007

KEE M. TUNG
SUPERVISORY PATENT EXAMINER